Improvements to Performance of Spiral Inductors on Insulators

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Abstract — **The performance of spiral inductors on insulating substrates is far superior to ones fabcricated in bulk CMOS or BiCMOS processes. Inspite of this, SOI inductors are generally not satisfactory for very low noise or low insertion loss circuits. This work studies high frequency effects on current density in inductors and discusses improvements in metallization and layout. Based on this research, a 5.5 nH inductor has been fabricated on sapphire with a 540 um diameter and 4.5 um thick aluminum, resulting in a quality factor of 25 at 2 GHz.**

I. INTRODUCTION

A great deal of research has been conducted on the modeling and improvement of inductors on both lightly doped and heavily doped silicon subtrates. The quality factor of these inductors is not limited by the conductivity of the metal turns themselves, but rather the amount of energy dissipated in the substrate. Losses manifest themselves as high series resistance due to magnetically coupled eddy currents and electrically coupled displacement currents in the substrate, and low self-resonant frequency f_{SR} due to the capacitance between the metal traces and the conductive substrate.

Despite the many efforts to improve the performance of inductors through ground shields, thick metal, and increased distance from the substrate, inductors fabricated on silicon rarely have a quality factor greater than ten, and are generally limited to below five [1]. To limit the losses induced by the substrate, most RF-focused processes provide a thick top-metal layer to build inductors.

The second order effects on quality factor in a silicon substrate technology are regularly ignored, but are the primary loss mechanisms in inductors on an insulating substrate. The quality factor of an inductor on an insulator is limited by current constriction due to skin effect, and more importantly the proximity effect of adjacent turns. The f_{SR} of inductors on insulators is usually several times the intended operating frequency and needs no improvement.

The next section describes the resistance increase in inductors due to the skin effect caused by self-inductance. Section III discusses the more deleterious proximity effect caused by the magnetic fields from adjacent turns and methods for mitigating this effect.

II. SKIN EFFECT

As the frequency of a wave guided by a conductor increases, the effective cross-sectional area of the conductor is reduced as time-varying fields attenuate quickly within a good conductor. The result is higher current density at the skin of the conductor and no current in the center of the conductor. The depth at which the current density has declined to e^{-1} is defined as the skin depth,

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \qquad (1)$$

In a semi-infinite conductor, there is virtually zero current density a few skin depths below the surface. Today, most semiconductor processes use aluminum for metal routing which has a conductivity of ~3.65×10^7 (S/m). Fig. 1 shows the skin depth versus frequency for aluminum.

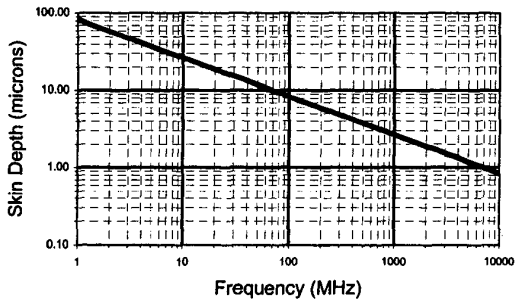

Fig. 1. Skin depth versus frequency of aluminum

Note the skin depth in the operating region of today's consumer products, e.g. 1 – 5 GHz. In this band, the skin depth of aluminum ranges from 2.63 um to 1.18 um. In order to minimize the ohmic losses in a conductor, a metal thickness should be chosen such that it is at least two skin depths thick at the operating frequency of interest. Fig. 2 shows the effective resistance versus frequency of a 10x400 um trace for both 1 um and 6 um thick aluminum. At 800 MHz, the 6 um thick metal is two skin depths thick. Past this frequency, the conductor resistance scales proportionally to the square root of operating frequency.

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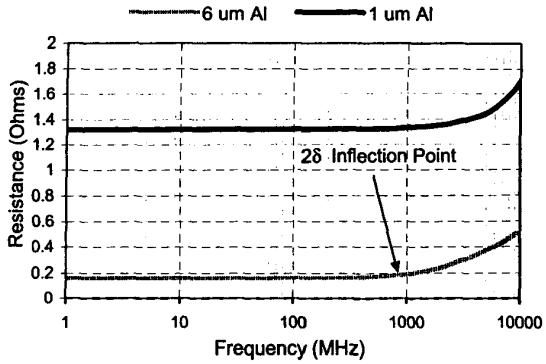

Fig. 2. Skin effect -- Resistance vs frequency

Choosing a metal thickness such that the inductor is operating past the 2δ point ensures that the resistance is limited by skin effect losses and not merely DC sheet resistance. Further, the thicker metal provides lower sheet rho for low frequency operation.

III. PROXIMITY EFFECT

While the skin effect increases resistance with the square-root of frequency, the proximity to adjacent turns in a spiral inductor causes resistance to increase with the square of frequency – a far more pronounced effect. The cause of this is the superposition of magnetic fields from all of the turns in the inductor creating eddy currents in each turn which crowds the desired current to one edge of the conductor. At the center of the spiral inductor, current is crowded at the inside edge of the metal. Conversely, at the outside of the inductor, the current is confined to the outer edge of the metal. Fig. 3 shows a current density plot for an inductor with significant proximity effect current crowding.

To combat this problem, the magnetic flux density in the inductor must be reduced. The inductor can either be physically larger in exchange for added cost, or the spacing between the turns can be increased at the expense of the turn width so that the total B-field normal to the conductors is lower. Prior work [2] has shown that increasing the spacing between turns extends the frequency range before the resistance takes on a square-law increase,

$$f_{critical} \propto \frac{Pitch}{Width^2} R_{sheet} \qquad (2)$$

If process changes are available, thickening the metal increases the cross-sectional area created by the metal height and the effective metal width due to the crowding effect. Metal spacing can also be increased while maintaining the same DC resistance. This method poses practical implementation problems as metal spacing rules increase with metal thickness, and metal deposition methods for ICs do not lend themselves well to very thick metal.

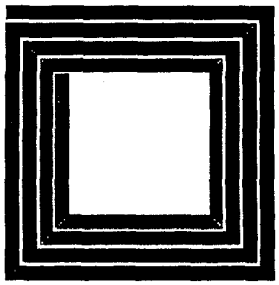

Fig. 3. Current crowding in an inductor at 2 GHz simulated with ASITIC [3]. The highest current density is black.

IV. RESULTS

Measured performance of the same inductor on silicon and sapphire substrates shows that thick metallization on insulator holds great promise for high-quality inductors. Table I summarizes the improvement in quality factor due to the insulating substrate and increased metal thickness.

TABLE I
Q of a 5.5 nH Circular Spiral Inductor on Si and Sapphire Subtrates

Substrate	Metallization	Rs (2 GHz)	Q (2 GHz)
20 Ω-cm Si	5.5 um Al	6.91	10
Sapphire	2.5 um Al	4.61	15
Sapphire	4.5 um Al	2.76	25

Shown in Fig. 4, the circular spiral inductor has a diameter of 540 um, turn width of 30 um, and turn spacing of 10 um.

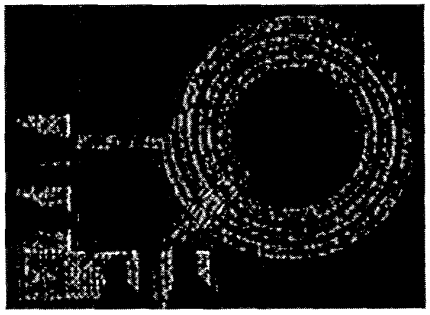

Fig. 4. Microphotograph of the 5.5 nH high-quality inductor.

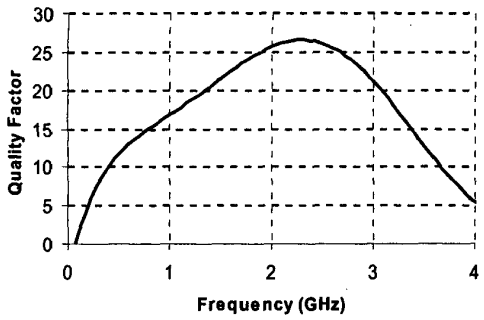

Fig. 5. Quality factor of the 4.5 um thick inductor.

Measured quality factor versus frequency of the 4.5 um thick inductor on sapphire is shown in Fig. 5. Work is underway to increase the metal thickness further from 4.5 um to 7.5 um to yield even higher quality factors.

V. CONCLUSION

RF circuits require passive elements for their operation, and noise requirements command the need for very low series resistance in inductors and thus high quality factors. For example, typical CMOS LNAs require an inductor in series with the input gate to achieve 50 Ω impedance matching. Parasitic resistance in the inductor adds directly to the noise figure of the LNA. Even an inductor series-resistance of only 3 Ω can lead to a 0.25 dB increase in noise figure, unacceptable when designing a 1.5 dB noise figure LNA. As gate lengths shrink, parasitic resistance in the series-matching inductor must remain constant for low noise operation, but inductance must increase to negate the MOS input capacitance, requiring higher quality factors.

In order to build low insertion loss passive networks such as filters and power splitters, RLC networks can be built on glass substrates to achieve quality factors in excess of 50. However, integrating these high performance networks into silicon subtrate ICs is not possible due to subtrate losses. SOI technologies such as silicon-on-sapphire open the door to fully monolithic RF circuits due to their inductors approaching the quality of discrete components.

ACKNOWLEDGEMENT

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